**LSM6DS33 – inertial module: 3D Accelerometer and 3D gyroscope**

**Summaries, Notes and links**

ST Link:

<https://www.st.com/en/mems-and-sensors/lsm6ds33.html>

Datasheet from above link



[Adafruit module information page](https://learn.adafruit.com/lsm6ds33-6-dof-imu=accelerometer-gyro)

[Adafruit module product page](https://www.adafruit.com/product/4485)

[SparkFun LSM6DS3 Hookup Guide](https://learn.sparkfun.com/tutorials/lsm6ds3-breakout-hookup-guide/all)

Features:

SPI or I2C serial interface

8 kbyte data buffering – possibility to store timestamp?

Event-detection interrupts – free -fall

Diagram, schematic

Description automatically generated

**Table

Description automatically generated**

Important to note:

Chip power supply VDDIO: Max. 3.7v

SCL I2C serial clock + SDA serial data

SA0 LSB of SAD

To select I2C, the CS line must be tied high (ie. Connected to Vdd\_IO)

Acceleration sensor and gyroscope, default power-down

**I2C Information**

[UM10204 – I2C-bus specification and user manual](https://www.nxp.com/docs/en/user-guide/UM10204.pdf)

There are two signals associated with the I2C bus: the serial clock line (SCL) and the Serial Data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd\_IO through external pull-up resistors. When the bus is free, both the lines are high.

Open drain, pull up resistors needs to be attached to high, devices are active low (eg 2k ohms for 400 kbps and 10k for 100 kbps)

A picture containing text

Description automatically generated

**I2C operation (from datasheet of Accelerometer)**

* The transaction on the bus is started through a START (ST) signal.

(A START condition is defined as a HIGH to LOW transition on the data line while SCL line is held HIGH)

(After this has been transmitted by the master, the bus is considered busy)

* The next byte of data transmitted after start condition contains address of the slave in the first 7 bits and the 8 bit specifies whether it is a Read (master is receiving data) or Write (master is transmitting data to slave)

(when address is sent, each device in the system compares first 7 bits after a start condition with its address. If they match the device considers itself addressed by the master.)

The Slave ADdress (SAD) associated to the LSM6DS33 is 110101xb. The SDO/SA0 pin can be used to change LSB of device address (x, b is to specify binary number).

Data transfer with acknowledge is mandatory. Transmitter must release SDA line during acknowledge pulse. Receiver must pull data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse.

A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

* After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub address (SUB) is transmitted.

(The increment of the address is configured by CTRL3\_C (12H\_ (IF\_INC))

* The slave address is completed with a Read/Write bit. If the bit is ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged

*Table 11* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations

Table

Description automatically generated

Table

Description automatically generated

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. (unlimited bytes transferred per transfer).

(Data transferred with the MSF first)

* If a receiver can’t receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line.

If a slave receiver doesn’t acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) data line must be left HIGH by the slave. The master can then abort transfer.

* A LOW TO HIGH transition on the SDA line while SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.
* In the presented communication format MAK is Master AcKnowledge and NMAK is No Master AcKnowledge.

**Arduino quick setup test code and libraries**

[LSM6 library for Arduino](https://github.com/pololu/lsm6-arduino#lsm6-library-for-arduino)

[Adafruit LSM6DS33 + LIS3MDL 9-DoF IMU with Accel/Gyro/Mag PCB](https://github.com/adafruit/Adafruit-LSM6DS33-LIS3MDL-PCB)

[Adafruit LSM6DS33 6-DoF Accel+Gyro IMU PCB](https://github.com/adafruit/Adafruit-LSM6DS33-PCB)

[Adafruit LSM6DS](https://github.com/adafruit/Adafruit_LSM6DS)

[SparkFun LSM6DS3 Arduino Library](https://github.com/sparkfun/SparkFun_LSM6DS3_Arduino_Library)

[brianClaus/LSM6DS33](https://os.mbed.com/users/bclaus/code/LSM6DS33/file/4e7d663e26bd/LSM6DS33.h/)